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<u>AbstractPlus</u> | Full Text: <u>PDF</u>(200 KB)   **IEEE CNF**

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Johansson, A.J.; Floberg, H.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium
Volume 5, 30 May-2 June 1999 Page(s):407 - 409 vol.5
<u>AbstractPlus</u> | Full Text: <u>PDF</u>(216 KB)   **IEEE CNF**

☐ 3. **Robust FPGA intellectual property protection through multiple small watermarks**
Lach, J.; Mangione-Smith, W.H.; Potkonjak, M.;
Design Automation Conference, 1999. Proceedings. 36th
21-25 June 1999 Page(s):831 - 836
<u>AbstractPlus</u> | Full Text: <u>PDF</u>(636 KB)   **IEEE CNF**

☐ 4. **An efficient implementation of the digital signature algorithm**
Kitsos, P.; Sklavos, N.; Koufopavlou, O.;
Electronics, Circuits and Systems, 2002. 9th International Conference on
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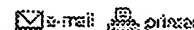**Search Results**   BROWSE   SEARCH   IEEE XPLORE GUIDE   SUPPOI

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☐ 1. **Digital signature proposal for mixed-signal circuits**
Brosa, A.M.; Figueras, J.;
Test Conference, 2000. Proceedings. International
3-5 Oct. 2000 Page(s):1041 - 1050

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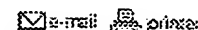Search Results   BROWSE   SEARCH   IEEE XPLORE GUIDE   SUPPOF

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Zervos, N.A.; Cupo, R.L.;
Communications, IEEE Transactions on
Volume 43, Issue 7, July 1995 Page(s):2184 - 2200
AbstractPlus | Full Text: PDF(1392 KB)   **IEEE JNL**

☐ 2. **A 300-MHz 115-W 32-b bipolar ECL microprocessor**
Jouppi, N.P.; Boyle, P.; Dion, J.; Doherty, M.J.; Eustace, A.; Haddad, R.W.; Mayo, R.; Menon, S.
Monier, L.M.; Stark, D.; Turrini, S.; Yang, J.L.; Hamburgen, R.; Fitch, J.S.; Kao, R.;
Solid-State Circuits, IEEE Journal of
Volume 28, Issue 11, Nov. 1993 Page(s):1152 - 1166
AbstractPlus | Full Text: PDF(1572 KB)   **IEEE JNL**

☐ 3. **Switched-capacitor simulation models for full-chips verification**
Chanak, T.; Chadha, R.; Singhal, K.;
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Volume 11, Issue 11, Nov. 1992 Page(s):1363 - 1371
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Micro, IEEE
Volume 10, Issue 3, June 1990 Page(s):22 - 35
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☐ 6. **On-wafer verification of a large-signal MESFET model**
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☐ 7. **System-on-a-chip verification--methodology and techniques**
Ferrari, F.;

Circuits and Devices Magazine, IEEE
Volume 18, Issue 6, Nov. 2002 Page(s):39 - 39

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☐ 8. **NOISY: an electrical noise checker for ULSI**
Gourdy, F.; Greiner, A.; Guillemet, M.; Marbot, R.; Murzin, J.;
Computer-Aided Design, 1988. ICCAD-88. Digest of Technical Papers., IEEE International Confe
- on
7-10 Nov. 1988 Page(s):226 - 229

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☐ 9. **Switched-capacitor simulation models for full-chip verification**
Chanak, T.; Chadha, R.; Singhal, K.;
Custom Integrated Circuits Conference, 1989., Proceedings of the IEEE 1989
15-18 May 1989 Page(s):21.1/1 - 21.1/4

AbstractPlus | Full Text: PDF(280 KB)   **IEEE CNF**

☐ 10. **Built-in test methodology for a full custom processor chip**
Shergill, R.S.; Yeung, P.-H.; Tucci, P.A.;
Computer Design: VLSI in Computers and Processors, 1989. ICCD '89. Proceedings., 1989 IEEI
International Conference on
2-4 Oct. 1989 Page(s):571 - 575

AbstractPlus | Full Text: PDF(408 KB)   **IEEE CNF**

☐ 11. **Integrated programmable operational amplifiers with improved characteristics**
Michael, S.; Cristi, R.;
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29 May-1 June 1990 Page(s):74 - 79

AbstractPlus | Full Text: PDF(352 KB)   **IEEE CNF**

☐ 12. **The design and verification of a VLSI chip for electrocardiogram data compression**
Roy, S.C.; Krakow, W.T.; Sacks, B.; Batchelor, W.E.; Bohs, L.N.; Barr, R.C.;
Computer-Based Medical Systems, 1990., Proceedings of Third Annual IEEE Symposium on
3-6 June 1990 Page(s):170 - 177

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☐ 13. **Linearity, accuracy and bandwidth considerations in wideband CMOS voltage amplifiers**
Ramirez-Angulo, J.; Sadkowski, R.; Sanchez-Sinencio, E.;
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on
3-6 May 1993 Page(s):1251 - 1254 vol.2

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☐ 14. **Design of a high complexity superscalar microprocessor with the portable IDPS ASIC libr**
Greiner, A.; Lucas, L.; Wajsburt, F.; Winckel, L.;
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☐ 15. **Stray insensitive implementation of programmable switched capacitor amplifiers**
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AbstractPlus | Full Text: PDF(280 KB)   **IEEE CNF**

☐ 16. **An efficient subcircuit extraction algorithm by resource management**
Zong Ling; Yun, D.Y.Y.;
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21-24 Oct. 1996 Page(s):9 - 14

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☐ **17. Optical probing of internal signals in silicon ICs**
De Venuto, D.; Corsi, F.; Breglio, G.; Cutolo, A.; Zeni, L.;
Electrotechnical Conference, 1996. MELECON '96., 8th Mediterranean
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De Venuto, D.; Corsi, F.;
Instrumentation and Measurement Technology Conference, 1996. IMTC-96. Conference Procee‹
'Quality Measurements: The Indispensable Bridge between Theory and Reality'., IEEE
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☐ **19. On the complexity of bridging fault simulation techniques for CMOS integrated circuits**
Ryan, C.A.;
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18-22 Sept. 1995 Page(s):160 - 163

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☐ **20. Bridging fault simulation using Iddq, logic, and delay testing**
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AUTOTESTCON '95. 'Systems Readiness: Test Technology for the 21st Century'. Conference R
8-10 Aug. 1995 Page(s):176 - 180

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☐ **21. The results of the VLSI implementation of high performance switched-capacitor analog bu
blocks**
Michael, S.;
Circuits and Systems, 1995., Proceedings., Proceedings of the 38th Midwest Symposium on
Volume 1, 13-16 Aug. 1995 Page(s):182 - 185 vol.1

AbstractPlus | Full Text: PDF(320 KB)   **IEEE CNF**

☐ **22. SUBTRACT: a program for the efficient evaluation of substrate parasitics in integrated cir‹**
Verghese, N.K.; Allstot, D.J.;
Computer-Aided Design, 1995. ICCAD-95. Digest of Technical Papers., 1995 IEEE/ACM Interna
Conference on
5-9 Nov. 1995 Page(s):194 - 198

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☐ **23. ECCOPUNCH: the Edinburgh classical conditioning pulsed neural chip**
Lehmann, T.;
Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on
Volume 1, 9-12 June 1997 Page(s):33 - 36 vol.1

AbstractPlus | Full Text: PDF(408 KB)   **IEEE CNF**

☐ **24. A symbolic simulation-based ANSI/IEEE Std 1149.1 compliance checker and BSDL genera**
Singh, H.; Patankar, G.; Beausang, J.;
Test Conference, 1997. Proceedings., International
1-6 Nov. 1997 Page(s):256 - 264

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☐ **25. Design and application of ATM-SDH multiplex/demultiplex ASIC**
Zhi Jun; Wei Shaojun; Chen Hongyi;
Communication Technology Proceedings, 1998. ICCT '98. 1998 International Conference on
22-24 Oct. 1998 Page(s):27 - 31 vol.1

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☐ **26. Word-level decision diagrams, WLCDs and division**
Scholl, C.; Becker, B.; Weis, T.M.;
Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers. 1998 IEEE/ACM Internat Conference on
8-12 Nov. 1998 Page(s):672 - 677
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☐ **27. Full-chip verification of UDSM designs**
Saleh, R.; Overhauser, D.; Taylor, S.;
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☐ **28. Full-chip verification methods for DSM power distribution systems**
Steele, G.; Overhauser, D.; Rochel, S.; Hussain, S.Z.;
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☐ **29. A new control method for dimmable high-frequency electronic ballasts**
Ribarich, T.J.; Ribarich, J.J.;
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Volume 3, 12-15 Oct. 1998 Page(s):2038 - 2043 vol.3
AbstractPlus | Full Text: PDF(388 KB)   **IEEE CNF**

☐ **30. A system-level co-verification environment for ATM hardware design**
Post, G.; Muller, A.; Grotker, T.;
Design, Automation and Test in Europe, 1998., Proceedings
23-26 Feb. 1998 Page(s):424 - 428
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☐ **31. A multi-megabit memory compiler: tomorrow's IP [integrated processor]**
Xian-Quan Zhang; Tsang, T.; Mehta, D.;
Electrical and Computer Engineering, 1999 IEEE Canadian Conference on
Volume 1, 9-12 May 1999 Page(s):538 - 542 vol.1
AbstractPlus | Full Text: PDF(496 KB)   **IEEE CNF**

32. A new control IC for dimmable high-frequency electronic ballasts

☐   Adams, J.; Ribarich, T.J.; Ribarich, J.J.;
Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual
Volume 2, 14-18 March 1999 Page(s):713 - 719 vol.2

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☐   33. **Optimization of a piezoelectric crystal driver stage using system simulations**
Johansson, J.;
Ultrasonics Symposium, 2000 IEEE
Volume 2, 22-25 Oct. 2000 Page(s):1049 - 1054 vol.2

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☐   34. **Compact modular expandable analog defuzzifiers using multiple input floating gate transi transconductance multipliers**
Ramirez-Angulo, J.; Choi, S.C.; Zrilic, J.Z.;
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International
Symposium on
Volume 5, 28-31 May 2000 Page(s):381 - 384 vol.5

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☐   35. **A hardware and software monitor for high-level system-on-chip verification**
El Shobaki, M.; Lindh, L.;
Quality Electronic Design, 2001 International Symposium on
26-28 March 2001 Page(s):56 - 61

AbstractPlus | Full Text: PDF(582 KB)   IEEE CNF

☐   36. **Simulation of on-chip interconnection effects in CMOS circuits**
Piwowarska, E.;
CAD Systems in Microelectronics, 2001. CADSM 2001. Proceedings of the 6th International
Conference. The Experience of Designing and Application of
12-17 Feb. 2001 Page(s):246 - 249

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☐   37. **The RF interface circuits design of contactless IC cards**
Lu Chao; Li Yong-ming;
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☐   38. **GSTE through a case study [digital IC verification]**
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☐   39. **VeriCDF: a new verification methodology for charged device failures**
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☐   40. **A wideband linear amplitude modulator for polar transmitters based on the concept of interleaving delta modulation**
Nagle, P.J.; Burton, D.P.; Heaney, E.P.; McGrath, F.J.;
Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE Internatio
Volume 1, 3-7 Feb. 2002 Page(s):296 - 467 vol.1

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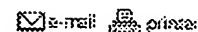
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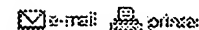Search Results   BROWSE   SEARCH   IEEE XPLORE GUIDE   SUPPOF

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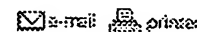BROWSE   SEARCH   IEEE XPLORE GUIDE   SUPPOF

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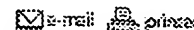Search Results   **BROWSE**   **SEARCH**   **IEEE XPLORE GUIDE**   **SUPPOF**

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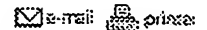**BROWSE**   **SEARCH**   **IEEE XPLORE GUIDE**   **SUPPOF**

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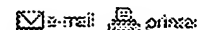**Search Results**   BROWSE   SEARCH   IEEE XPLORE GUIDE   SUPPOF

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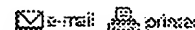
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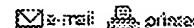::::Search Results   BROWSE   SEARCH   IEEE XPLORE GUIDE   SUPPOF

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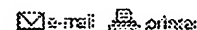Search Results   BROWSE   SEARCH   IEEE XPLORE GUIDE   SUPPOF

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Lee, T.C.; Tibel, D.; Sullivan, T.D.; Forhan, S.;
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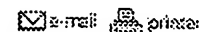
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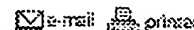BROWSE   SEARCH   IEEE XPLORE GUIDE   SUPPOF

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☐   **2. Dynamic life-estimation of CMOS ICs in real operating environment: precise electrical met and MLE**
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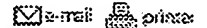**Welcome United States Patent and Trademark Office**

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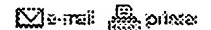**Inspec**

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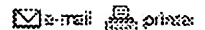Inspec

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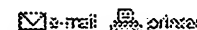Search Results   BROWSE   SEARCH   IEEE XPLORE GUIDE   SUPPOF

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